

8T95, 96, 97, 98 Hex Buffers/Inverters

High Speed Hex 3-State Buffers
High Speed Hex 3-State Inverters
Product Specification

Logic Products

DESCRIPTION

Each of the 3-state bus interface elements described herein has low current PNP inputs and is designed with Schottky TTL technology for ultra high speed. The devices are used to convert TTL/DTL or MOS/CMOS to 3-state TTL bus levels. For maximum systems flexibility, the 8T95 and 8T97 do so without logic inversion, whereas the 8T96 and 8T98 provide the logical complement of the input. The 8T95 and 8T96 feature a common control line for all six devices, whereas the 8T97 and 8T98 have control lines for four devices from one input and two from another input.

FUNCTION TABLE — 8T95

INPUTS			OUTPUT
DIS ₁	DIS ₂	I	Y
L	L	L	L
L	L	H	H
X	H	X	(Z)
H	X	X	(Z)

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance (off) state

FUNCTION TABLE — 8T96

INPUTS			OUTPUT
DIS ₁	DIS ₂	I	\bar{Y}
L	L	L	H
L	L	H	L
X	H	X	(Z)
H	X	X	(Z)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
N8T95	8ns	65mA
N8T96	6.5ns	59mA
N8T97	8ns	65mA
N8T98	6.5ns	59mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N8T95N, N8T96N N8T97N, N8T98N
Plastic SO	N8T97N, N8T98D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	8T
DIS	Input	1Sul
I	Input	1Sul
Y	Output	24Sul

NOTE:

A unit load (Sul) is $50\mu A$ I_{IH} and $-2.0mA$ I_{IL} .

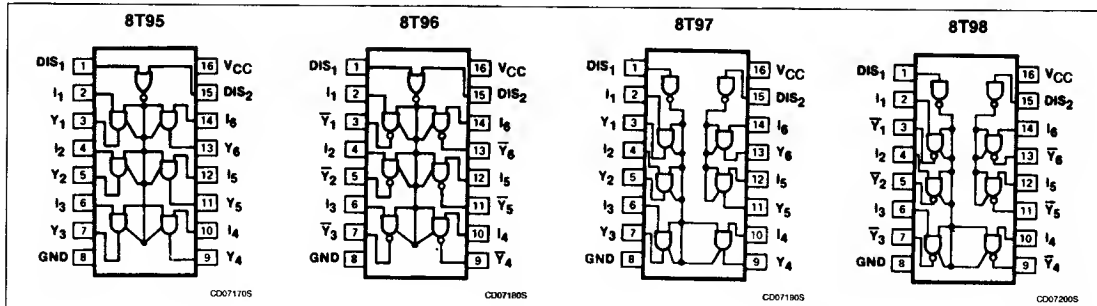
FUNCTION TABLE — 8T97

INPUTS		OUTPUT
DIS	I	Y
L	L	L
L	H	H
H	X	(Z)

FUNCTION TABLE — 8T98

INPUTS		OUTPUT
DIS	I	\bar{Y}
L	L	H
L	H	L
H	X	(Z)

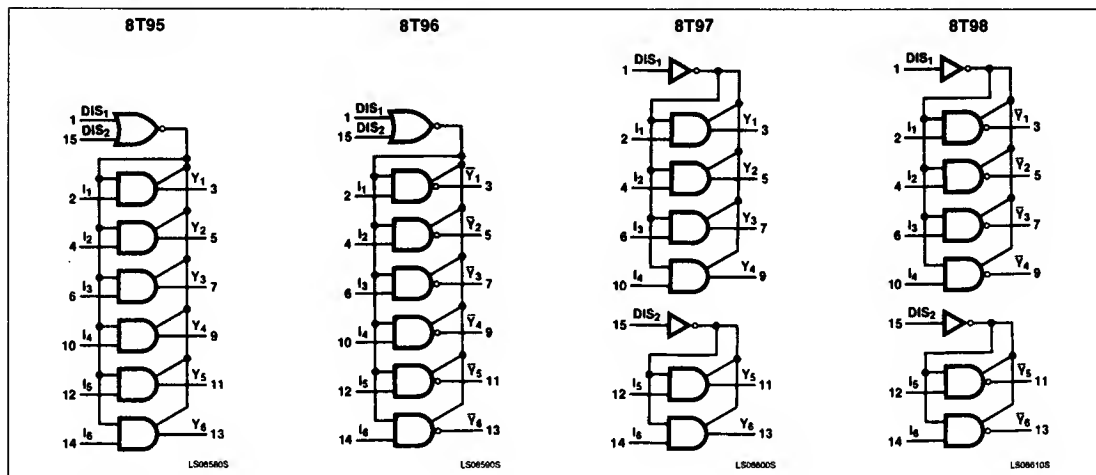
PIN CONFIGURATION



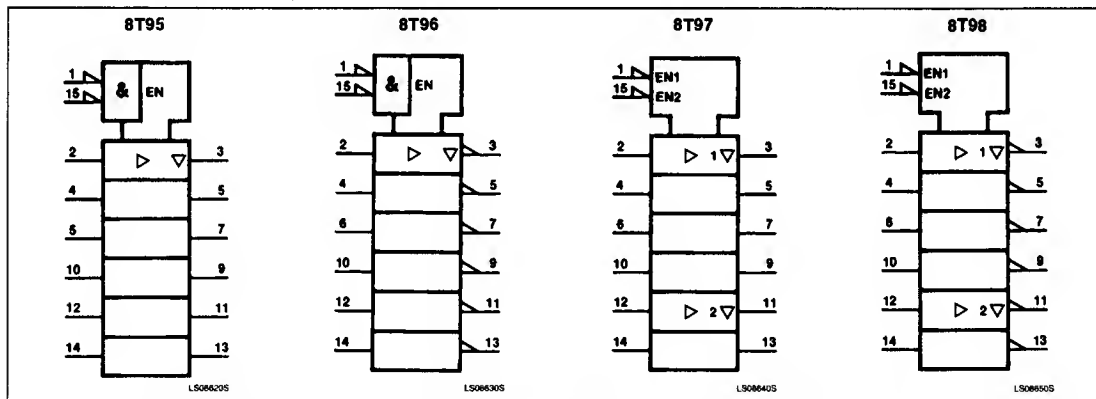
Hex Buffers/Inverters

8T95, 96, 97, 98

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	S8T	N8T	UNIT
V_{CC} Supply voltage	7.0	7.0	V
V_{IN} Input voltage	-0.5 to +5.5	-0.5 to +5.5	V
I_{IN} Input current	-30 to +5	-30 to +5	mA
I_{OL} Continuous	100	100	mA
V_{OUT} Voltage applied to output in HIGH output state	-0.5 to V_{CC}	-0.5 to V_{CC}	V
T_A Operating free-air temperature range	-55 to +125	0 to 70	°C

8T95, 96, 97, 98

TEST CIRCUIT

Input Characteristics
 $V_A = 3V$, $f = 1MHz$, $t_r = t_f < 10ns$ (10% to 90%)
 C_L includes probe and jig capacitance.

PARAMETER	TEST CONDITIONS ¹		8T95/97		8T96/98		UNIT
			Min	Max	Min	Max	
V _{IH} Input HIGH voltage	Guaranteed input HIGH threshold voltage		2.0		2.0		V
V _{IL} Input LOW voltage	Guaranteed input LOW threshold voltage			0.8		0.8	V
V _{IK} Input clamp diode voltage	V _{CC} = MIN, I _{IK} = -12mA			-1.5		-1.5	V
V _{BD} Input breakdown voltage	V _{CC} = MAX, I _I = 1mA		5.5		5.5		V
V _{OH} HIGH-level output voltage	V _{CC} = MIN, I _{OH} = -5.2mA		2.4		2.4		V
V _{OL} LOW-level output voltage	V _{CC} = MIN, I _{OL} = 48mA			0.5 ³		0.5 ³	V
I _{OZH} Off-state output current, HIGH-level voltage applied	V _{CC} = MAX, V _O = 2.4V			40		40	μA
I _{OZL} Off-state output current, LOW-level voltage applied	V _{CC} = MAX, V _O = 0.5V			-40		-40	μA
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.4V			40		40	μA
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.5V	Disable = 0.5V		-400		-400	μA
		Disable = 2.0V		-40		-40	μA
I _{OS} Short-circuit output current ²	V _{CC} = MAX		-40	-115	-40	-115	mA
I _{CC} Supply current (total)	V _{CC} = MAX			98		89	mA

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. I_{OS} is tested with $V_{OUT} = +0.5V$ and $V_{CC} = V_{CC\ MAX} + 0.5V$. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
3. $V_{OL} = +0.45V\ MAX$ for S8T at $T_A = +125^\circ C$ only.

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8T95, 96, 97, 98

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER		TEST CONDITIONS	8T95/97		8T96/98		UNIT
			R _L = 200Ω		R _L = 200Ω		
			Min	Max	Min	Max	
t _{PLH}	Propagation delay Data inputs to data outputs	S ₁ , S ₂ are closed, C _L = 50pF		12		11	ns
t _{PHL}	Propagation delay Data inputs to data outputs	S ₁ , S ₂ are closed, C _L = 50pF		13		10	ns
t _{PZH}	Disable to outputs High Z to logic "1"	S ₁ is open, S ₂ is closed, C _L = 50pF		25		22	ns
t _{PZL}	Disable to outputs High Z to logic "0"	S ₁ is closed, S ₂ is open, C _L = 50pF		25		24	ns
t _{PHZ}	Disable to outputs Logic "1" to high Z	S ₁ , S ₂ are closed, C _L = 5pF		10		10	ns
t _{PLZ}	Disable to outputs Logic "0" to high Z	S ₁ , S ₁ are closed, C _L = 5pF		12		16	ns

AC WAVEFORMS

